Listing of the Claims:

1. (Previously Presented) An in-plane switching liquid crystal display device comprising:

first and second substrates;

a gate line and a data line defining a pixel region on the first substrate;

a first conductive line formed directly on the first substrate;

a common line on the first conductive line;

a thin film transistor at a crossing portion between the gate and data lines;

a plurality of pixel electrodes on the first substrate;

a plurality of common electrodes on the first substrate;

a first pixel electrode connecting line on the first substrate; and

a liquid crystal layer between the first and second substrates.

2. (Original) The device of claim 1, wherein the first pixel electrode connecting line is partially overlapped with the common line.

3. (Original) The device of claim 1, further comprising an auxiliary pattern extended from the first conductive line.

4. (Currently Amended) The device of claim 3, wherein the auxiliary pattern is between the data line and the first pixel electrode connecting line.

5. (Original) The device of claim 3, wherein the auxiliary pattern is formed outermost of the common electrodes.

6. (Original) The device of claim 1, further comprising a second conductive line underneath the gate line.

7. (Original) The device of claim 1, wherein the thin film transistor includes gate, source and drain electrodes.

8. (Original) The device of claim 7, wherein the common electrode is at the same layer as the gate electrode.

9. (Original) The device of claim 7, wherein the pixel electrode is at the same layer as the source and drain electrodes.

10. (Previously Presented) An in-plane switching liquid crystal display device comprising:

first and second substrates;

a gate line and a data line defining a pixel region on the first substrate;

a first conductive line formed directly on the first substrate;

a common line on the first conductive line;

a thin film transistor at a crossing portion between the gate and data lines;

a plurality of pixel electrodes on the first substrate;

a plurality of common electrodes on the first substrate;

an auxiliary pattern extended from the first conductive line; and

a liquid crystal layer between the first and second substrates.

11. (Original) The device of claim 10, further comprising a first pixel electrode connecting line on the first substrate.

12. (Original) The device of claim 11, wherein the first pixel electrode connecting line is partially overlapped with the common line.

13. (Currently Amended) The device of claim 11, wherein the auxiliary pattern is between the ~~first conductive~~ data line and the first pixel electrode connecting line.

14. (Original) The device of claim 10, wherein the auxiliary pattern is formed outermost of the common electrodes.

15. (Original) The device of claim 10, further comprising a second conductive line underneath the gate line.

16. (Original) The device of claim 10, wherein the thin film transistor includes gate, source and drain electrodes.

17. (Original) The device of claim 16, wherein the common electrode is at the same layer as the gate electrode.

18. (Original) The device of claim 16, wherein the pixel electrode is at the same layer as the source and drain electrodes.

19. (Previously Presented) A method for fabricating an in-plane switching liquid crystal display device comprising:

forming a gate line and a data line defining a pixel region on a first substrate;

forming a first conductive line directly on the first substrate;

forming a common line on the first conductive line;

forming a thin film transistor at a crossing portion between the gate and data lines;

forming a plurality of pixel electrodes on the first substrate;

forming a plurality of common electrodes on the first substrate;

forming a first pixel electrode connecting line on the first substrate; and

forming a liquid crystal layer between the first substrate and a second substrate facing the first substrate.

20. (Original) The method of claim 19, wherein the first pixel electrode connecting line is partially overlapped with the common line.

21. (Original) The method of claim 19, further comprising forming an auxiliary pattern extended from the first conductive line.

22. (Currently Amended) The method of claim 21, wherein the auxiliary pattern is between the data line and the first pixel electrode connecting line.

23. (Original) The method of claim 19, wherein the auxiliary pattern is formed outermost of the common electrodes.

24. (Previously Presented) The method of claim 19, further comprising forming a second conductive line underneath the gate line.

25. (Original) The method of claim 19, wherein the thin film transistor includes gate, source and drain electrodes.

26. (Previously Presented) The method of claim 25, wherein the common electrode is formed at the same layer as the gate electrode.

27. (Previously Presented) The method of claim 25, wherein the plurality of pixel electrodes are at the same layer as the source and drain electrodes.